We claim:

1. An interconnection system for a plurality of processing elements (PEs), each PE having a communications port for transmitting and receiving data and commands, the interconnection system comprising:

inter-PE connection paths; and

a cluster switch connected to said PEs so as to combine mutually exclusive inter-PE connection paths and to thereby substantially reduce the number of communications paths required to provide inter-PE connectivity equivalent to that of conventional torus-connected PE arrays.

2. The interconnection system of claim 1, wherein said cluster switch further comprises connections to provide direct communications between transpose PEs.

3. The interconnection system of claim 1, wherein data and commands may be transmitted and received at said communications ports in one of four selectable modes:

a) transmit east/receive west mode for transmitting data to an east PE via the communications port while receiving data from a west PE via the communications port;

b) transmit north/receive south mode for transmitting data to a north PE via the communications port while receiving data from a south PE via the communications port;

c) transmit south/receive north mode for transmitting data to an south PE via the communications port while receiving data from a north PE via the communications port; and

d) transmit west/receive east mode for transmitting data to a west PE via the communications port while receiving data from an east PE via the communications port.

4. The interconnection system of claim 3, wherein data and commands may be transmitted and received in a fifth selectable, transpose transmit/receive, mode for transmitting

and receiving between transpose PEs.

5. The interconnection system of claim 4, further comprising a controller and memory system connected to the PEs to simultaneously send control information to each PE's control port and to send data to each PE's data port for loading into registers at each PE.

6. The interconnection system of claim 5, wherein said inter-PE connection paths are selectively switched by path enabling signals.

7. The interconnection system of claim 5, wherein said path enabling signals are generated based upon control information from said controller.

8. The interconnection system of claim 4, wherein each communication port includes B-bit wide transmission and reception paths, where B is an integer greater than or equal to one.

9. The interconnection system of claim 1, wherein each PE is connected to selectively send commands or data over a communications port while receiving data or commands via another communications port, based upon communications instructions received through the control port and decoded in the control logic residing on each of the PEs.

10. The interconnections system of claim 9, wherein the communication instruction is received by the control logic from a controller over said control port.

11. The interconnection system of claim 9, wherein the cluster switch supports an operation wherein the PEs are each simultaneously sending commands or data while receiving commands or data.

12. The interconnections system of claim 11, wherein said simultaneous operation is selectively switched such that the PEs are each simultaneously sending commands or data while receiving data or instructions.

13. An array processor, comprising:

a plurality of processing elements (PEs), each PE having a single inter-PE communications port; and

inter-PE communications paths connected to provide inter-PE connectivity equivalent to that of a conventional torus connected array.

14. The array processor of claim 13, further comprising inter-PE communications paths connected to provide direct transpose PE communications.

15. An array processor, comprising:

a plurality of processing elements (PEs) arranged in clusters;

inter-PE communications paths connected such that the PEs of each cluster communicate in mutually exclusive directions with the PEs of each of at least two other clusters; and

cluster switches connected to multiplex inter-PE communications in said mutually exclusive directions.

16. An array processor, comprising:

N clusters of M processing elements, each processing element having a communications port through which the processing element transmits and receives data over a total of B wires;

communications paths which are less than or equal to (M)(B)-wires wide connected between pairs of said clusters; each cluster member in the pair containing processing elements which are torus nearest neighbors to processing elements in the other

cluster of the pair, each path permitting communications between said cluster pairs in two mutually exclusive torus directions, that is, South and East or South and West or North and East or North and West; and

multiplexers connected to combine 2(M)(B)-wire wide communications into said less than or equal to (M)(B)-wires wide paths between said cluster pairs.

17. The array processor of claim 16, wherein the processing elements of each cluster communicate to the North and West torus directions with one cluster and to the South and East torus directions with another cluster.

18. The array processor of claim 16, wherein the processing elements of each cluster communicate to the North and East torus directions with one cluster and to the South and West torus directions with another cluster.

19. The array processor of claim 16, wherein at least one cluster includes an N x N torus transpose pair.

20. The array processor of claim 16, wherein a cluster switch comprises said multiplexers and said cluster switch is connected to mutliplex communications received from two mutually exclusive torus directions to processing elements within a cluster.

21. The array processor of claim 20, wherein said cluster switch is connected to multiplex communications from the processing elements within a cluster for transmission to another cluster.

22. The array processor of claim 21, wherein said cluster switch is connected to multiplex communications between transpose processing elements within a cluster.

23. The array processor of claim 16, wherein N is greater than or equal to M.

24. The array processor of claim 16, wherein N is less than M.

25. An array processor, comprising:

N clusters of M processing elements, each processing element having a communications port through which the processing element transmits and receives data over a total of B wires and each processing element within a cluster being formed in closer physical proximity to other processing elements within a cluster than to processing elements outside the cluster;

communications paths which are less than or equal to (M)(B)-wires wide connected between pairs of said clusters, each cluster member in the pair containing processing elements which are torus nearest neighbors to processing elements in the other cluster of the pair, each path permitting communications between said cluster pairs in two mutually exclusive torus directions, that is, South and East or South and West or North and East or North and West; and

multiplexers connected to combine 2(M)(B)-wire wide communications into said less than or equal to (M)(B)-wires wide paths between said cluster pairs.

26. The array processor of claim 25, wherein the processing elements of each cluster communicate to the North and West torus directions with one cluster and to the South and East torus directions with another cluster.

27. The array processor of claim 25, wherein the processing elements of each cluster communicate to the North and East torus directions with one cluster and to the South and West torus directions with another cluster.

28. The array processor of claim 25, wherein at least one cluster includes an N x N torus transpose pair.

29. The array processor of claim 25, wherein a cluster switch comprises said multiplexer and said cluster switch is connected to mutliplex communications received from two mutually exclusive torus directions to processing elements within a cluster.

30. The array processor of claim 29 wherein said cluster switch is connected to multiplex communications from the processing elements within a cluster for transmission to another cluster.

31. The array processor of claim 30, wherein said cluster switch is connected to multiplex communications between transpose processing elements within a cluster.

32. The array processor of claim 25, wherein N is less than or equal to M.

33. The array processor of claim 25, wherein N is greater than M.

34. The array processor of claim 25, wherein communications between processing elements is bit-serial and each processing element cluster communicates with two other clusters over said communications paths.

35. The array processor of claim 25, wherein the communications paths between processing elements comprise a data bus.

36. The array processor of claim 25, wherein said communications paths are bidirectional paths.

37. The array processor of claim 25, wherein said communications paths comprise unidirectional signal wires.

38. The array processor of claim 25, wherein P and Q are the number of rows and columns, respectively, of a torus connected array having the same number of PEs as said array, and P and Q are equal to N and M, respectively.

39. The array processor of claim 25, wherein P and Q are the number of rows and columns, respectively, of a torus connected array having the same number of PEs and P and Q are equal to M and N, respectively.

40. An array processor, comprising:

processing elements (PEs) $PE_{i,j}$, where i and j refer to the respective row and column PE positions within a conventional torus-connected array, and where i = 0,1,2, ... N-1 and j = 0, 1, 2, . . . N-1, said PEs arranged in clusters $PE_{(i+a)(ModN),(j+N-a)(ModN)}$, for any i,j and for all a $\in$ {0,1,...,N-1}; and

cluster switches connected to multiplex inter-PE communications paths between said clusters thereby providing inter-PE connectivity equivalent to that of a torus-connected array.

41. The array processor of claim 40, wherein said cluster switches are further connected to provide direct communications between PEs in a transpose PE pair within a cluster.

42. The array processor of claim 40, wherein said clusters are scaleable.

43. A method of forming an array processor, comprising the steps of:

arranging processing elements in N clusters of M

processing elements, such that each cluster includes processing elements which communicate only in mutually exclusive torus directions with the processing elements of at least one other cluster; and

multiplexing said mutually exclusive torus direction communications.